LIQUID CRYSTAL DISPLAY AND FABRICATING METHOD THEREOF

Fig. 1 A1

A17

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to a liquid crystal display and fabricating method thereof, and more particularly to a liquid crystal display that obtains the capacitance of a storage capacitor while increasing the aperture ratio.

Description of the Related Art

[0002] Generally, a liquid crystal display (LCD) controls the light transmittance of liquid crystal cells in response to a video signal to thereby display a picture. An active matrix LCD having a switching device for each liquid crystal cell is suitable for displaying a moving picture. The active matrix LCD mainly uses a thin film transistor (TFT) as the switching device.

[0003] The LCD uses a storage capacitor for the purpose of sustaining the voltage drop across the liquid crystal to assure the stability of a gray level display. The storage capacitor is classified into a storage on gate (SOG) system that overlaps a portion of the (n-1)th gate line with the nth pixel electrode to form a storage capacitor of the nth pixel, and a storage on common (SOC) system that provides a separate common electrode at the lower portion of a pixel electrode to form a storage capacitor.

[0004] Fig. 1 is a plan view showing a structure of an array substrate of a conventional LCD adopting a storage on gate system, and Fig. 2 is a section view of the array substrate taking along the A-A' line in Fig. 1.

[0005] Referring to Fig. 1 and Fig. 2, a lower substrate 11 of the LCD includes a TFT arranged at an intersection between a gate line 15' and a data line 17. A pixel electrode 33 is connected to a drain electrode 27 of the TFT, and a storage capacitor is positioned at an overlapping portion between the pixel electrode 33 and the pre-stage gate line 15.

[0006] The TFT includes a gate electrode 13 connected to the gate line 15', a source electrode 25 connected to the data line 17, and a drain electrode 27 connected, via a first contact hole 30a, to the pixel electrode 33. Further, the TFT includes a gate insulating film 19 for insulating the gate electrode 13 and the source and drain electrodes 25 and 27, and semiconductor layers 21 and 23 for defining a conduction channel between the source electrode 25 and the drain electrode 27 by a gate voltage applied to the gate electrode 13. Such a TFT responds to a gate signal from the gate line 15' to selectively apply a data signal from the data line 17 to the pixel electrode 33.

[0007] The pixel electrode 33 is positioned at a cell area divided by the data line 17, and the gate line 15' and is made from a transparent conductive material having a high light transmittance. The pixel electrode 33 is provided on a protective film 31 coated on the entire surface of the lower substrate 11 and is electrically connected, via the first contact hole 30a defined in the protective film 31, to the drain electrode 27. The pixel electrode 33 generates a potential difference from a common transparent electrode (not shown) provided at an upper substrate (not shown) by a data signal applied via the TFT. This potential difference allows a liquid crystal positioned between the lower substrate 11 and the upper substrate (not shown) to change

the liquid crystalline molecular arrangement in accordance with its dielectric anisotropy. Accordingly, an arrangement of the liquid crystal molecules is changed for each pixel in accordance with a data voltage applied via the TFT, thereby expressing pictorial information on the LCD.

[0008] The storage capacitor should have a capacitance value large enough to maintain a stable pixel voltage. To this end, the storage capacitor includes a capacitor electrode 29 electrically connected, via a second contact hole 30b, to the pixel electrode, and a gate line 15 having a gate insulating film 19 therebetween.

[0009] Fig. 3A to Fig. 3E are section views for explaining a method of fabricating the array substrate of the LCD shown in Fig. 2.

[0010] Referring first to Fig. 3A, the gate electrode 13 and the gate line 15 are provided on the substrate 11. The gate electrode 13 and the gate line 15 are formed by depositing aluminum (A1), copper (Cu) or other suitable materials by using a deposition technique such as sputtering, and then patterning it.

[0011] Referring to Fig. 3B, the gate insulating film 19, an active layer 21 and an ohmic contact layer 23 are provided. The gate insulating film 19 is formed by depositing an insulating material such as silicon nitride (SiN_X) or silicon oxide (SiO_X) using a plasma enhanced chemical vapor deposition (PECVD) technique in such a manner as to cover the gate electrode 13 and the gate line 15.

[0012] The active layer 21 and the ohmic contact layer 23 are formed by sequentially disposing two semiconductor layers on the gate insulating film 19 and then patterning the disposed semiconductor layers. The active layer 21 is formed from amorphous silicon that is not doped

with an impurity. On the other hand, the ohmic contact layer 23 is formed from amorphous silicon doped with an n-type or p-type impurity at a high concentration.

[0013] Referring to Fig. 3C, the data line 17, the source and drain electrodes 25 and 27 and the capacitor electrode 29 are provided on the gate insulating film 19. The data line 17, the source and drain electrodes 25 and 27 and the capacitor electrode 29 are formed by entirely depositing a metal layer using a CVD technique or a sputtering technique and then patterning. After the source and drain electrodes 25 and 27 were patterned, the ohmic contact layer 23 at an area corresponding to the gate electrode 13 is patterned to expose the active layer 21. The area of the active layer 21 corresponding to the gate electrode 13 between the source and drain electrodes 25 and 27 makes a channel. The capacitor electrode 29 overlaps with the gate line 15. The data line 17, the source and drain electrodes 25 and 27 and the capacitor electrode 29 are made from chromium (Cr) or molybdenum (Mo).

[0014] Referring to Fig. 3D, a protective layer 31 having first and second contact holes 30a and 30b is provided. The protective layer 31 is formed by depositing an insulating material on the gate insulating layer 19 and then patterning it in such a manner to cover the source and drain electrodes 25 and 27. The protective layer 31 is mainly made from an inorganic insulating material such as silicon nitride (SiN_X) or silicon oxide (SiO_X).

[0015] Referring to Fig. 3E, a pixel electrode 33 is provided on the protective film 31. The pixel electrode 33 is formed by depositing a transparent conductive material on the protective film 31 and then patterning it. The pixel electrode 33 is electrically connected, via the first

contact hole 30a, to the drain electrode 27 and is electrically connected, via the second contact hole 30b, to the capacitor electrode 29. The pixel electrode 33 is made from a transparent conductive material that can be indium-tin-oxide (ITO), indium-zinc-oxide (IZO) or indium-tin-zinc-oxide (ITZO).

[0016] Fig. 4 is a plan view showing a structure of an array substrate of a conventional LCD having storage on a common system. Fig. 5 is a sectional view of the array substrate taking along the B-B' line in Fig. 4.

[0017] In this storage on common system, a storage capacitor 50 is positioned at the center of a pixel area. The storage capacitor 50 should have a capacitance value large enough to maintain a stable pixel voltage. To this end, the storage capacitor 50 has a pixel electrode 55 electrically connected to a drain electrode 59, and a capacitor common electrode 45 having a gate insulating film 49 therebetween.

[0018] Fig. 6A to Fig. 6D are section views for explaining the method steps of fabricating the array substrate of the LCD shown in Fig. 5.

[0019] Referring to Fig. 6A, the gate electrode 43, the capacitor electrode 45 and the gate line 47 are provided on the substrate 41. The gate electrode 43, the capacitor electrode 45 and the gate line 47 are formed by depositing aluminum (A1), copper (Cu) or other suitable material by using a deposition technique, preferably sputtering, and then patterning.

[0020] Referring to Fig. 6B, the gate insulating film 49, an active layer 51 and an ohmic contact layer 53 are provided. The gate insulating film 49 is formed by depositing an insulating material such as silicon nitride

(SiN_X) or silicon oxide (SiO_X) using a plasma enhanced chemical vapor deposition (PECVD) technique so as to cover the gate electrode 43, the capacitor common electrode 45 and the gate line 47.

[0021] The active layer 51 and the ohmic contact layer 53 are formed by sequentially disposing two semiconductor layers on the gate insulating film 49 and then patterning the disposed semiconductor layers. The active layer 51 is formed from undoped amorphous silicon. On the other hand, the ohmic contact layer 53 is formed from amorphous silicon doped with a high concentration of an N-type or P-type impurity.

[0022] Referring to Fig. 6C, a pixel electrode 55, the data line 63 and source and drain electrodes 57 and 59 are provided on the gate insulating film 49. The pixel electrode 55 is formed by depositing a transparent conductive material on the gate insulating film 49 and then patterning it. The pixel electrode 55 is made from any one of ITO, IZO and ITZO.

[0023] Subsequently, the data line 63 (see Fig. 4) and the source and drain electrodes 57 and 59 are provided. The data line 63 and the source and drain electrodes 57 and 59 are formed by entirely depositing a metal layer using a CVD technique or a sputtering technique and then patterning. After the source and drain electrodes 57 and 59 were patterned, the ohmic contact layer 53 at an area corresponding to the gate electrode 43 is patterned to expose the active layer 51. The area of the active layer 51 corresponding to the gate electrode 43 between the source and drain electrodes 57 and 59 makes a channel. The drain electrode 59 electrically contacts the pixel electrode 55 without any contact hole. The data line 63 and the source

and drain electrodes 57 and 59 are made from chromium (Cr) or molybdenum (Mo).

[0024] Referring to Fig. 6D, a protective film 61 is provided at a TFT area. The protective film 61 forms by depositing an insulating material on the gate insulating layer 19 and then patterning it in such a manner to cover the source and drain electrodes 57 and 59. The protective film 61 is mainly made from an inorganic insulating material such as silicon nitride (SiN_X) or silicon oxide (SiO_X).

[0025] Such a liquid crystal display has an increased capacitance value of the storage capacitor so as to overcome the flicker phenomenon. Increasing the capacitance value of the storage capacitor requires increasing the area of the capacitor electrode. In other words, the LCD of storage on gate system should widen the width of the gate line so as to increase the capacitance value of the storage capacitor. However, since the aperture ratio is reduced and a line delay effect of a gate signal is enhanced when a width of the gate line is widened, there is a limit to widening the width of the gate line. Furthermore, since the LCD of storage on common system has the storage capacitor provided at the center of the pixel cell, this LCD has a smaller aperture ratio than a LCD of a storage on gate system.

[0026] As discussed above, as the area of the capacitor electrode increases, the aperture ratio is reduced. In particular, a high pixel density LCD, a ferroelectric LCD or a semi-ferroelectric LCD acquires high capacitance value of the storage capacitor while greatly reducing the aperture ratio. However, modern display technology requires enhanced capacitance while simultaneously maintaining or increasing the aperture ratio.

SUMMARY OF THE INVENTION

[0027] Accordingly, it is an object of the present invention to provide a liquid crystal display and a fabricating method thereof that is capable of increasing the capacitance of a storage capacitor while increasing aperture ratio.

[0028] The invention, in part, pertains to a liquid crystal display that includes a gate electrode and a gate line to which a scanning signal is supplied, a gate insulating film entirely deposited on a substrate to cover the gate electrode, an active layer formed on the gate insulating film to overlap with the gate electrode, an ohmic contact layer formed on the active layer, a source electrode formed on the ohmic contact layer, a drain electrode formed on the ohmic contact layer and opposed to the source electrode so as to have a channel in between them. A protective layer is formed on the entire surface of a substrate to cover the source and the drain electrodes, and a data line crosses with the gate line and connects to the source electrode in the manner of piercing the protective layer. A storage electrode is formed at a pixel cell area of the same layer as the gate electrode and the gate line, and a pixel electrode is formed to oppose to the storage electrode having the gate insulating film in between them and electrically connected with the drain electrode.

[0029] In a liquid crystal display of a preferred embodiment of the invention, a contact hole connects the source electrode with the data line. The liquid crystal display can further include a buffer metal layer on the source and the drain electrodes for reducing contact resistance. The buffer metal layer is formed of one of molybdenum (Mo), titanium (Ti) or tantalum (Ta). In the

liquid crystal display, the storage electrode is formed of a transparent conductive material such as indium tin oxide (ITO). The liquid crystal display can further include a auxiliary storage electrode connected to each storage electrode.

[0030] The invention, in part, pertains to a method of fabricating a liquid crystal display that includes the steps of forming a gate electrode and a gate line on a substrate and at the same time forming a storage electrode on the same layer where the gate electrode and the gate line are formed, forming a gate insulating film to cover the gate electrode, the gate line and the storage electrode, forming an active layer on the gate insulating film to overlap with the gate electrode, forming an ohmic contact layer on the active layer, forming a source electrode and a drain electrode by patterning to expose the active layer, forming a protective layer on the source electrode and the drain electrode, forming a contact hole that pierces the protective layer, and forming a data line crossed with the gate line and connected with the source electrode through the contact hole.

[0031] The method according to a preferred embodiment of the invention further includes the step of forming a buffer metal layer on the source electrode and the drain electrode for reducing contact resistance. The buffer metal layer can be formed of one of molybdenum (Mo), titanium (Ti) or tantalum (Ta). In the method, the storage electrode is formed of a transparent conductive material such as indium tin oxide (ITO). In the method, an auxiliary storage electrode is formed to connect the storage electrode. The protective layer can be an organic insulating material of at least one material selected from

the group consisting of acrylics, polytetrafluoroethylene, benzocyclobutene, perfluoropolymer resin and perfluorocyclobutane.

[0032] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0033] The accompanying drawings are included to provide a further understanding of the invention. The drawings illustrate embodiments of the invention and together with the description serve to explain the principles of the embodiments of the invention.

[0034] Fig. 1 is a plan view illustrating an array substrate of a conventional liquid crystal display having a storage on gate (SOG) system;

[0035] Fig. 2 is a sectional view of the array substrate, shown in Fig. 1, taken along the line A-A';

[0036] Fig. 3a to Fig. 3e are sectional views representing by steps a method of fabricating the array substrate shown in Fig. 2;

[0037] Fig. 4 is a plan view illustrating an array substrate of a conventional liquid crystal display having a storage on common (SOC) system;

[0038] Fig. 5 is a sectional view of the array substrate, shown in Fig. 4, taken along the line B-B';

[0039] Fig. 6a to Fig. 6d are sectional views representing steps of a method of fabricating the array substrate shown in Fig. 5;

[0040] Fig. 7 is a plan view illustrating an array substrate of a liquid crystal display according to a first embodiment of the present invention;

[0041] Fig. 8 is a sectional view of the array substrate, shown in Fig. 7, taken along the line C-C';

[0042] Fig. 9 to Fig. 14 are sectional views representing steps of a method of fabricating the array substrate shown in Fig. 8;

[0043] Fig. 15 is a plan view illustrating an array substrate of a liquid crystal display according to a second embodiment of the present invention;

[0044] Fig. 16 is a sectional view of the array substrate, shown in Fig. 15, taken along the lines D-D', E-E', F-F'; and

[0045] Fig. 17 to Fig. 22 are sectional views representing by steps a method of fabricating the array substrate shown in Fig. 16.

DETAILED DESCRIPTION

[0046] Advantages of the present invention will become more apparent from the detailed description given herein after. However, it should be understood that the detailed description and specific examples, while indicating preferred embodiments of the invention, are given by way of illustration only, since various changes and modifications within the spirit and scope of the invention will become apparent to those skilled in the art from this detailed description.

[0047] Fig. 7 to Fig. 22 illustrate preferred embodiments of the present invention.

[0048] Fig. 7 is a plan view illustrating an array substrate of a liquid crystal display according to a first

embodiment of the present invention, and Fig. 8 is a sectional view of the array substrate, shown in Fig. 7, taken along the line.

[0049] Referring to Fig. 7 and Fig. 8, a lower substrate 71 includes a TFT positioned at an intersection of a gate line 74 and a data line 91. A pixel electrode 87 connects to a drain electrode 85 of the TFT and a storage capacitor positioned at a pixel cell area.

[0050] The TFT includes a gate electrode 73 connected to the gate line 74, a source electrode 83 connected with the data line 91 through a contact hole 90a, and a drain electrode 85. Further, the TFT includes a gate insulating film 77 for insulating the gate electrode 73 from the source and drain electrodes 83 and 85, and an active layer 79 and an ohmic contact layer 81 for forming a channel between the source electrode 83 and the drain electrode 85 by a gate voltage supplied to the gate electrode 73. Here, the source and the drain electrodes 83 and 85 have metal layers 83a and 85a and buffer metal layers 83b and 85b. The buffer metal layer 85b of the drain electrode 85 connects with the pixel electrode 87 without using a contact hole. The data line 91 electrically connects to the buffer metal layer 83b of the source electrode 83 through the contact hole 90a formed at a protective layer 89. The TFT responds to a gate signal from the gate line 74 and supplies a data signal from the data line 91 to the pixel electrode 87 through the source electrode 83 and the drain electrode 85 connected with the data line 91.

[0051] The pixel electrode 87 is positioned at the cell area divided by the data line 91 and the gate line 74. The pixel electrode 87 is made of a transparent conductive material having good light transmissivity, such as ITO. The

pixel electrode 87 generates a potential difference from a common transparent electrode (not shown) by the data signal supplied via the TFT. The liquid crystal located between the lower substrate 71 and an upper substrate switches by the dielectric anisotropy interacting with the potential difference, whereby light incident from a light source is transmitted.

[0052] The storage capacitor is charged with a voltage during the period when a gate high voltage is applied to the gate line 74, and discharges the charged voltage during the period when the data signal is supplied to the pixel electrode 87, thereby preventing a voltage swing of the pixel electrode 87. The volume of the storage capacitor should be large enough to stabilize the pixel voltage. For this, the storage electrode 75 is formed at the lower part of the pixel electrode 87 provided at the cell area, thereby increasing the capacitance.

[0053] Fig. 9 to Fig. 14 are sectional views illustrating by steps a method of fabricating the array substrate shown in Fig. 8, according to a preferred embodiment of the invention.

[0054] Referring to Fig. 9, the gate electrode and the storage electrode 75 which are projected from the gate line 74, are formed on the substrate 71.

[0055] The gate electrode 73 forms by depositing aluminum (Al) or copper (Cu) by, for example, a sputtering technique, followed by patterning. The aluminum or copper deposition is not restricted to sputtering, but any suitable deposition technique can be utilized.

[0056] The storage electrode 75 is formed by depositing a transparent conductive material that can be any one of ITO, IZO or ITZO, in the pixel area. A sputtering

technique or any other suitable deposition method can be used. Then the storage electrode 75 is patterned.

[0057] Referring to Fig. 10, the gate insulating film 77 is formed on the gate electrode 73 and the storage electrode 75. The active layer 79 and the ohmic contact layer 81 are formed on the gate insulating film 77.

[0058] The gate insulating film 77 is formed by covering the gate electrode 73 and the storage electrode 75. The gate insulating film 77 is formed of an insulating material such as silicon nitride SiN_X, silicon oxide SiO_X or other suitable material by a plasma enhanced chemical vapor deposition (PECVD) technique.

[0059] The active layer 79 and the ohmic contact layer 81 are formed by depositing two semiconductor layers on the gate insulating film 77 and then patterning them. The active layer 79 is formed of undoped amorphous silicon, and the ohmic contact layer 81 is formed of amorphous silicon in which N-type or P-type impurities are doped in high concentration.

[0060] Fig. 11 shows the formation of the source and the drain electrodes.

[0061] The source and the drain electrodes 83 and 85 are composed of metal layers 83a and 85a and buffer metal layers 83b and 85b.

[0062] The metal layers 83a and 85a are formed by depositing aluminum (Al) or copper (Cu) over the gate insulating film 77 by a CVD technique or a sputtering technique.

[0063] The buffer metal layers 83b and 85b are formed by entirely depositing on the metal layers 83a and 85b. Here, molybdenum (Mo), titanium (Ti), tantalum (Ta) or any suitable metal that has good conductivity are used as

the buffer metal layers 83b, 85b for reducing the contact resistance of the metal layers 83a, 85a. The source and the drain electrodes 83 and 85 are formed by patterning metal layers 83a and 85a and buffer metal layers 83b and 85b. Thereafter, the corresponding part of the ohmic contact layer 81 to the gate electrode 73 is patterned to expose the active layer 79. The corresponding part of the active layer 79 of the gate electrode 73 between the source and the drain electrodes 83 and 85 becomes a channel.

[0064] Subsequently, the pixel electrode 87 is formed on the gate insulating film 77, as is shown in Fig. 12.

[0065] The pixel electrode 87 is formed by depositing a transparent conductive material, e.g., one of ITO, IZO and ITZO, and then patterning it. The pixel electrode 87 is electrically in contact with the buffer metal layer 85b of the drain electrode 85.

[0066] Referring to Fig. 13, the contact hole 90a is formed on the protective layer 89.

[0067] The protective layer 89 is formed by coating an insulating material by a spin coating technique to cover the source and drain electrodes 83 and 85. Accordingly, the surface of the protective layer 79 is flattened. In the protective layer 79 is formed the contact hole 90a which is patterned and in which the buffer metal layer 83b of the source electrode 83 is exposed.

[0068] The protective layer 79 is formed of an organic insulating material, having a small dielectric constant, such as an acrylic organic compound, TEFLON (polytetrafluoroethylene) , benzocyclobutene (BCB), CYTOP (perfluoropolymer resin), perfluorocyclobutane (PFCB), etc.

[0069] Referring to Fig. 14, the data line 91 is formed on the protective layer 89.

[0070] The data line 91 is formed by depositing aluminum (Al), copper (Cu) or any other suitable material by, for example, a sputtering technique, followed by patterning. The data line 91 is electrically connected with the buffer metal layer 83b of the source electrode 83 through the contact hole 90a.

[0071] Fig. 15 is a plan view illustrating an array substrate of a liquid crystal display according to a second preferred embodiment of the present invention, Fig. 16 is a sectional view of the array substrate, shown in Fig. 15, taken along the lines taken along the line D-D', E-E', F-F'.

[0072] Referring to Fig. 15 and Fig. 16, a lower substrate 101 includes a TFT located at the intersection of a gate line 104 and a data line 121 and a pixel electrode 117. The TFT connects to a drain electrode 115 and a storage capacitor located at a pixel cell area.

[0073] The TFT includes a gate electrode 103 connected to the gate line 104, a source electrode 113 connected with the data line 121 through a contact hole 120a, and a drain electrode 115. The TFT includes a gate insulating film 107 for insulating the gate electrode 103 from the source and drain electrodes 113 and 115, an active layer 109 and an ohmic contact layer 111 for forming a channel between the source electrode 113 and the drain electrode 115 by a gate voltage supplied to the gate electrode 103. Here, the source and the drain electrodes 113 and 115 are composed of metal layers 113a and 115a and buffer metal layers 113b and 115b. The data line 121 is electrically connected with the buffer metal layer 113b of the source electrode 113 through a contact hole 120a formed

at a protective layer 119. The TFT responds to a gate signal from the gate line 104 and electively supplies a data signal from the data line 121 to the pixel electrode 117.

[0074] The pixel electrode 117 is positioned at the cell area divided by the data line 121 and the gate line 104. The pixel electrode 117 is made of a transparent conductive material having good light transmissivity, such as ITO. The pixel electrode 117 is electrically connected with the buffer metal layer 115b of the drain electrode 115. The pixel electrode 117 generates a potential difference from a common transparent electrode by the data signal supplied via the TFT. The liquid crystal located between the lower substrate 101 and an upper substrate switches according to its dielectric anisotropy reacting to the potential difference. Light is transmitted according to the degree of the rotation of the liquid crystal.

[0075] The storage capacitor is charged with a voltage during the period when a gate high voltage is applied to the gate line 104, and discharges the charged voltage during the period when the data signal is supplied to the pixel electrode 117, thereby preventing a voltage swing of the pixel electrode 117. The storage capacity of the storage capacitor should be large enough to stabilize the pixel voltage. For this, the storage capacitor provides the storage electrode 105 at each corresponding pixel cell area corresponding to the pixel electrode 117. An auxiliary storage electrode 105A connects the storage electrode 105 formed at each pixel cell.

[0076] Fig. 17 to Fig. 22 are sectional views illustrating by steps a method of fabricating the array substrate shown in Fig. 16.

[0077] Referring to Fig. 17, the storage electrode 105 including the auxiliary storage electrode 105A and the gate electrode 103 connected with the gate line 104, are formed on the substrate 101.

[0078] The gate electrode 103 is formed by entirely depositing aluminum (Al), copper (Cu) or other suitable material by, for example, a sputtering technique, followed by patterning.

[0079] The storage electrode 105 is formed by depositing a transparent conductive material and then patterning it. The storage electrode 105 is formed of any one of ITO, IZO or ITZO.

[0080] The auxiliary storage electrode 105A is electrically connected by coupling the storage electrode 105 formed at each pixel cell.

[0081] Referring to Fig. 18, the active layer 109 and the ohmic contact layer 111 are formed on the gate insulating film 107.

[0082] The gate insulating film 107 is formed by entirely depositing on the substrate 101 an insulating material that can be, but is not restricted to, silicon nitride (SiN_X) or silicon oxide (SiO_X) by a plasma enhanced chemical vapor deposition (PECVD) technique so as to cover the gate electrode 103 and the storage electrode 105. The active layer 109 and the ohmic contact layer 111 are formed by depositing two semiconductor layers over the gate insulating film 107 and then patterning them. Here, the active layer 109 is formed of undoped amorphous silicon. The ohmic contact layer 111 is formed of amorphous silicon in which N-type or P-type impurities are doped at high concentration.

[0083] Referring to Fig. 19, the source and the drain electrodes 113 and 115 are formed. The source and the drain electrodes 113 and 115 are composed of metal layers 113a and 115a and buffer metal layers 113b and 115b.

[0084] The metal layers 113a and 115a are formed by depositing aluminum (A1) or copper (Cu) entirely over the gate insulating film 107 by a CVD technique or a sputtering technique. The buffer metal layers 113b and 115b are formed by entirely depositing on the metal layers 113a and 115a a highly conductive material such as molybdenum (Mo), titanium (Ti) or tantalum (Ta). Here, the buffer metal layers 113b and 115b are formed to reduce the contact resistance of the metal layers 113a and 115a. The source and the drain electrodes 113 and 115 are formed by patterning the metal layers 113a, 115a and buffer metal layers 113b, 115b. Afterwards, the part of the ohmic contact layer 111 corresponding to the gate electrode 103 is patterned to expose the active layer 109. The part of the active layer 109 corresponding to the gate electrode 103 between the source and the drain electrodes 113 and 115 become a channel.

[0085] Subsequently, the pixel electrode 117 is formed, as is shown in Fig. 20.

[0086] The pixel electrode 117 is formed by depositing a transparent conductive material on the gate insulating film 107 and then patterning it. The pixel electrode 117 is electrically in contact with the buffer metal layer 115b of the drain electrode 115. The pixel electrode 117 corresponds to the storage electrode 105 and is formed of any one of ITO, IZO or ITZO.

[0087] Referring to Fig. 21, a contact hole 120a is formed on the protective layer 119.

[0088] The protective layer 119 is formed by coating an insulating material by a spin coating technique to cover the source and drain electrodes 113 and 115. By patterning, the protective layer forms the contact hole 120a which exposes the buffer metal layer 113b of the source electrode 113.

[0089] The protective layer 109 is formed of an organic insulating material, having a small dielectric constant, such as acrylic organic compound, i.e., acrylics, TEFLON (polytetrafluoroethylene), benzocyclobutene (BCB), CYTOP (perfluoropolymer resin), perfluorocyclobutane (PFCB).

[0090] Referring to Fig. 22, the data line 121 is formed on the protective layer 119.

[0091] The data line 121 is formed by depositing aluminum (Al), copper (Cu) or other suitable material by a sputtering or other appropriate technique, followed by patterning. The data line 121 electrically connects with the buffer metal layer 113b of the source electrode 113 through the contact hole 120a.

[0092] Thus, in the liquid crystal display and the fabricating method thereof according to the present invention, the storage electrode of a transparent conductive material is formed at each pixel cell area. Also, the pixel electrode electrically connected with the buffer metal layer is formed by providing the buffer metal layer on the source and the drain electrodes. In this invention, the area of the storage capacitor is increased by the storage electrode and the pixel electrode. Accordingly, the aperture ratio increases and the capacitance of the capacitor increases.

[0093] As described above, the liquid crystal display and the fabricating method thereof according to the present invention increases the aperture ratio of the

storage capacitor and is capable of increasing the capacitance of the storage capacitor. As a result, in the present invention, the picture quality becomes uniform and stable owing to the high accuracy thereof.

[0094] It should be understood to a person having ordinary skill in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the scope and spirit of the invention. Accordingly, the scope of the invention shall be determined only by the appended claims and their equivalents.